AMENDMENTS TO THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1. (currently amended) A method of switching transactions on an interconnect switch, the interconnect switch having a primary port connected to a primary interconnect, a first secondary port connected to a bridge, and a plurality of end-device ports, each connectable to one of a plurality of end devices, the method comprising the steps of:

identifying a transaction from a primary port as a bridge transaction or a non-bridge transaction;

routing the bridge transaction to the bridge through the first secondary port;

routing the non-bridge transaction to at least one of the plurality of end device ports.

2. (original) The method of claim 1, wherein the transaction has a target address, the step of identifying a transaction as a bridge transaction or a non-bridge transaction comprising the steps of:

shadowing registers of the bridge with a plurality of shadow registers in the interconnect switch;

if the target address is mapped by the shadow registers, identifying the transaction as a bridge transaction; and

if the target address is not mapped by the shadow registers, identifying the transaction as a non-bridge transaction.

3. (original) The method of claim 2, the step of shadowing registers comprising the step of:

shadowing base address registers of the bridge in the switch, the base address registers of the bridge mapping addresses associated with a secondary interconnect of the bridge.

4. (original) The method of claim 2, the step of shadowing comprising the step of:

snooping a configuration transaction that configures base address registers of the bridge; and

copying base address register information obtained in the snooping step to the shadow registers.

5. (original) The method of claim 1, the step of routing a non-bridge transaction comprising the step of:

broadcasting the non-bridge transaction to each of the plurality of end-device secondary ports.

6. (original) The method of claim 1, the step of routing a non-bridge transaction comprising the step of:

successively routing the non-bridge transaction to each of the end-device secondary ports until the non-bridge transaction is claimed by a first end device connected to a first end-device secondary port.

7. (currently amended) The method of claim 6, wherein the non-bridge transaction has a target address, further comprising the steps of:

identifying an address range associated with the first end device;

routing further non-bridge transactions with the target address within the address range to the first end-device secondary port; and

successively routing further non-bridge transactions to each other of the plurality of end-device secondary ports until claimed by another end device.

8. (original) The method of claim 1, wherein the transaction is a peer-to-peer transaction.

9. (original) The method of claim 1, wherein the transaction is a downstream transaction.

10. (currently amended) An interconnect switch, comprising:

a primary port, ~~coupled to a primary interconnect~~configured to couple to a primary bus segment;

a switch engine coupled to the primary port;

a secondary-bridge port configured to couple to a secondary bus segment; and

one or more secondary-end-device ports each configured to couple to an end device;

~~a first interconnect bridge coupled to the primary port;~~

~~a secondary interconnect coupled to the first interconnect bridge;~~

~~a plurality of secondary ports coupled to the secondary interconnect, comprising:~~

~~a bridge port, coupled to a second interconnect bridge; and~~

~~a plurality of end-device ports, each coupled to one of a plurality of end devices;~~

wherein the ~~a~~ switch engine comprises~~, comprising~~:

circuitry to receive a transaction, the transaction having a target address;

circuitry to decode the target address;

circuitry to route the transaction to the secondary-bridge port if the circuitry to decode the target address decodes the target address as directed to the ~~second interconnect bridge~~secondary bus segment; and

circuitry to route the transaction to ~~the plurality of~~at least one of the one or more secondary-end-device ports if the circuitry to decode the target address decodes the target address as not directed to ~~the second interconnect bridge~~a bridge.

11. (currently amended) The interconnect switch of claim 10, wherein the circuitry to route the transaction to at least one of the ~~plurality of~~one or more secondary-end-device ports ~~comprising:~~comprises circuitry to broadcast the transaction to ~~the plurality of~~ a plurality of secondary-end-device ports.

12. (currently amended) The interconnect switch of claim 10, wherein the circuitry to route the transaction to at least one of the ~~plurality of~~ one or more end-device ports ~~comprising:~~comprises circuitry to successively route the transaction to each of the ~~plurality of~~one or more secondary-end-device ports until the transaction is claimed by ~~an~~a claiming end device.

13. (canceled)

14. (currently amended) The interconnect switch of ~~claim 13~~claim 12, wherein the circuitry to route transactions to at least one of the one or more secondary-end-device ports further ~~comprising~~comprises:

circuitry to store ~~the~~ an end-device address range associated with the claiming end device;

circuitry to route further transactions to the claiming end device if the target address is within the end-device address range.

15. (canceled).

16. (original) The interconnect switch of claim 10, wherein the transaction is a downstream transaction.

17. (original) The interconnect switch of claim 10, wherein the transaction is a peer-to-peer transaction.

18. (new) The interconnect switch of claim 10, comprising two or more secondary-end-device ports.

19. (new) A system, comprising:

a processor;

a memory coupled to the processor;

an interconnect bus coupled to the processor, the interconnect bus comprising:

a primary bus segment coupled to the processor;

a switch having a primary side with a primary port coupled to the primary bus segment and a secondary side with a plurality of secondary ports, the switch comprising a routing engine configured to selectively transmit a transaction from the primary port to at least one secondary-port of the plurality of secondary ports based on the absence of a bridge downstream from the at least one secondary-port.

20. (new) The system of claim 19, wherein the switch comprises:

a shadow register;

circuitry configured to snoop at least a portion of a target address of a transaction that passes through a bridge connected to one of the plurality of secondary ports; and

circuitry configured to compare the snooped portion of the target address with at least a portion of a target address of an unclassified transaction to identify the unclassified transaction as a non-bridge transaction.

21. (new) The system of claim 19, comprising a secondary bus segment coupled to one of the plurality of secondary ports and an end device coupled to another one of the secondary ports.

22. (new) The system of claim 19, wherein the switch comprises circuitry configured to store the snooped portion of the target address in a shadow register.